

AMENDMENTS TO THE CLAIMS

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1. (Currently Amended) A semiconductor memory device comprising:
a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer;
an invalid address detecting circuit for detecting that an address signal supplied from exterior indicates an address space other than said address space; and
an invalid signal outputting circuit for outputting an invalid signal to the exterior of the semiconductor memory device when said invalid address detecting circuit carries out said detection, thereby notifying a system unit accessing the semiconductor memory device of the detection.

2. (Original) A semiconductor memory device according to claim 1, comprising an output controlling circuit for outputting, when said invalid address detecting circuit carries out said detection in a read operation, a data signal read in a read operation cycle immediately preceding said read operation.

3. (Original) A semiconductor memory device according to claim 2, comprising an output circuit for receiving a read data signal from said memory cells and continuously outputting the received data to the exterior, according to a control by the output controlling circuit when said invalid address detecting circuit carries out said detection in said read operation.

4. (Original) A semiconductor memory device according to claim 1, comprising an output controlling circuit for giving high impedance to a data output terminal when said invalid address detecting circuit carries out said detection in a read operation.

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5. (Original) A semiconductor memory device comprising:
a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer;
an invalid address detecting circuit for detecting that an address signal supplied from exterior indicates an address space other than said address space; and
an output controlling circuit for outputting, when said invalid address detecting circuit carries out said detection in a read operation, a data signal read in a read operation cycle immediately preceding said read operation.

6. (Original) A semiconductor memory device according to claim 5, comprising an output circuit for receiving a read data signal from said memory cells and continuously outputting the received data to the exterior, according to a control by the output controlling circuit when said invalid address detecting circuit carries out said detection in said read operation.

7. (Currently Amended) A semiconductor memory device according to claim 1, further comprising:

~~a plurality of nonvolatile memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer;~~

~~a command controlling circuit for carrying out a write or an erase operation in said memory cells in response to a command input from the exterior; and, wherein~~

~~said command controlling circuit invalidates said command input to thereby prohibit the write or the erase operation, when the an invalid address detecting circuit for detecting detects that an the address signal supplied from the exterior as the command input indicates an the address space other than the said address space, wherein~~

~~the command input is invalidated when said invalid address detecting circuit carries out said detection.~~

8. (Cancelled)

9. (Currently Amended) A method of controlling a semiconductor memory device comprising a plurality of memory cells corresponding to an address space larger than 2^n and small than $2^{(n+1)}$, where n is a positive integer, said method comprising the step of:

outputting an invalid signal to exterior of the semiconductor memory device when an address signal supplied from the exterior indicating an address space other than said address space has been detected, thereby notifying a system unit accessing the semiconductor memory device of the detection.

10. (Currently Amended) A method of controlling a semiconductor memory device according to claim 9, further comprising a plurality of memory cells ~~corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer and the steps of:~~

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automatically carrying out a write or an erase operation in said memory cells in response to a command input from the exterior, ~~said method comprising the step of~~

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invalidating the command input thereby prohibiting the write or the erase operation, when an the address signal supplied from the exterior indicating an the address space other than the said address space has been detected.

11. (New) A semiconductor memory device according to claim 1, further comprising:

a decoder which decodes said address signal, and is inactivated when said invalid address detecting circuit carries out said detection.

12. (New) A semiconductor memory device according to claim 1, further comprising:

a sense amplifier which amplifies a data signal read from the memory cells, and is inactivated when said invalid address detecting circuit carries out said detection.